Model Answer

Sub: LIC & Its Application

Code: AS-4148

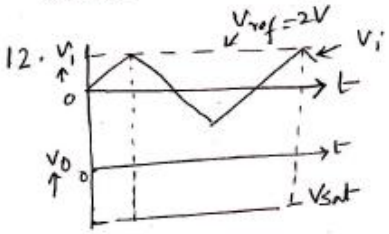
1. (b).
2. ∞
3. Triangular
4. Buffer is unity gain amplifier used for impedance matching and reducing loading effect.
5. 20dB/decade.
6. $+45^0$
7. $\frac{1}{2^n-1} \times 100\% = \frac{1}{2^4-1} \times 100\% = \frac{1}{15} \times 100\% = 6.67\%$
8. $V_o = \frac{V_1}{V_2}$
9. Switching Regulator
10. 50%
11. CMRR is a measure of a differential amplifier's capacity to eliminate common signals and is defined as $CMRR = \frac{\text{Diff. mode gain}}{\text{Common mode gain}}$. Higher the CMRR, better the differential amplifier is of eliminating common mode signal like noise etc. It is expressed in dB and $CMRR = 20\log_{10}\left(\frac{A_1}{A_C}\right)$. Value of CMRR is ∞ for ideal OPAMP.

Slew Rate is known as dynamic characteristics of OPAMP. It is the time rate of change of closed loop amp. o/p voltage under large signal condⁿ. It is also the fastest rate at which OPAMP o/p voltage can change. For ideal OPAMP, slew rate is ∞ and is expressed as slew rate $= \left.\frac{dV_o}{dt}\right|_{max}$ (V/μs). It changes with change in voltage gain and normally specified at unity gain and is measured by step i/p dc voltage.

Offset voltage – An ideal OPAMP is perfectly balanced when both i/ps are equal i.e. o/p = 0 when both i/p are equal. But a practical OPAMP exhibits an unbalance due to mismatch of internal circuitry and produced an error voltage and error currents at i/p and o/p terminals. This i/p offset voltage is the voltage that must be applied between i/p terminals of OPAMP to make o/p voltage to zero. For ideal OPAMP, i/p offset voltage is zero.

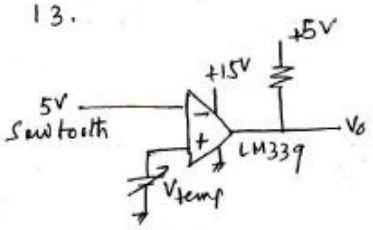
Unity gain bandwidth is the range of frequency of an OPAMP when the voltage gain is unity.

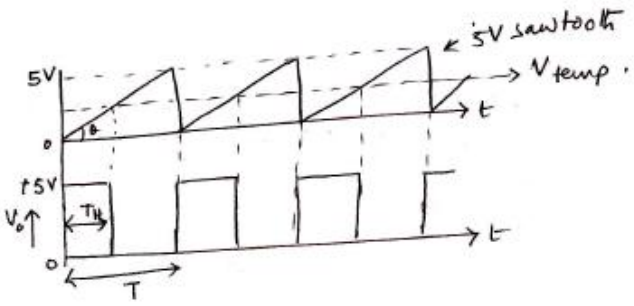
12.



Since the OPAMP is working in openloop cond^n and $V_i \leq V_{ref}$ at o/p will be $-V_{sat}$ as shown in the figure.

13.



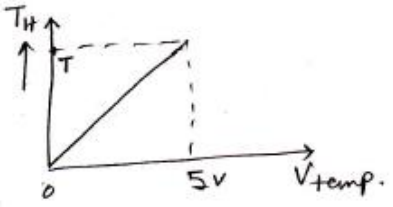


As seen from waveform, the on time pulse width T_H is changing directly with the ref. voltage level V_{temp}.

From similarity of trigonometric forms, we can write,

$$\tan\theta = \frac{V_{temp}}{T_H} = \frac{5V}{T}$$ where T = total pulse duration

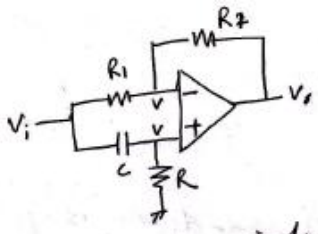
$$\therefore T_H = \frac{T}{5V} \times V_{temp}.$$ or $\boxed{T_H \propto V_{temp}.}$



At $V_{temp} = 0$, $T_H = 0$

At $V_{temp} = 5V$, $T_H = T$ = max^m value of T_H

14.



Due to the virtual ground, voltage at +ve i/p terminal will be same as that at -ve i/p terminal and we took the voltage as 'V'.

For +ve i/p terminal, we can write,

$$V = \frac{R}{R+\frac{1}{sC}} V_i = \frac{RSC\,V_i}{1+RSC} \quad ---(1)$$

For -ve i/p terminal, we can write,

$$\frac{V_i - V}{R_1} = \frac{V - V_0}{R_1}$$

or, $V_i + V_0 = 2V$ ---(2)

Putting the value of V from (1) to (2),

$$V_i + V_0 = \frac{2RSC}{1+RSC} V_i$$

or, $V_0 = V_i \left[\frac{2RSC - 1 - RSC}{1+RSC}\right]$

or, $V_0 = \frac{RSC-1}{RSC+1} V_i$

or, $\frac{V_0}{V_i}(s) = \frac{RSC-1}{RSC+1}$

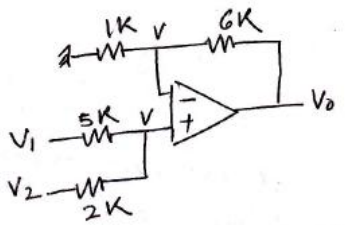
$$\frac{V_0}{V_i}(jw) = \frac{-jwRC-1}{-jwCR+1} \qquad \therefore \left|\frac{V_0}{V_i}(jw)\right| = \frac{\sqrt{w^2R^2C^2+1}}{\sqrt{w^2C^2R^2+1}} = 1$$

$$= \frac{(-jwRC-1)^2}{1+w^2C^2R^2}$$

$$= \frac{-1-w^2R^2C^2-2jwCR}{1+w^2C^2R^2} = \frac{-(1+w^2R^2C^2)-2jwCR}{1+w^2C^2R^2}$$

$$\therefore \angle\frac{V_0}{V_i}(jw) = -\tan^{-1}\left(\frac{-2wCR}{(1+w^2C^2R^2)}\right)$$

$$= 2\tan^{-1}(wCR)$$

15. 

$V_0 = 2V_1 + 5V_2$

Due to closed loop feedback, virtual ground ~~con~~ is applicable here and V = voltage at +ve input terminal = voltage at -ve input terminal

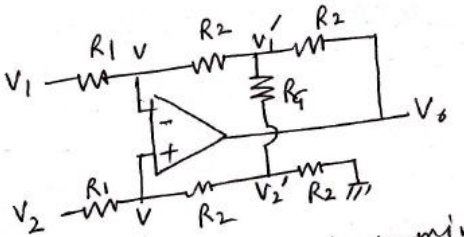
$$\therefore V = \frac{2K}{2K+5K} V_1 + \frac{5K}{2K+5K} V_2 = \frac{2V_1 + 5V_2}{7}$$

At -ve terminal, we can write,

$$\frac{0-V}{1K} = \frac{V-V_0}{6K} \quad \text{or,} \quad -6V = V - V_0$$

or, $V_0 = 7V$

or, $V_0 = 7 \times \left(\frac{2V_1 + 5V_2}{7}\right) = 2V_1 + 5V_2$

16. 

Due to virtual ground, V = voltage at -ve i/p terminal = voltage at +ve i/p terminal

Using KCL at -ve i/p terminal and at the point of V_1' shown in figure, we can write,

$$\frac{V_1 - V}{R_1} = \frac{V - V_1'}{R_2} = \frac{V_1' - V_2'}{R_4} + \frac{V_1' - V_0}{R_2} \quad \text{---(1)}$$

Using KCL at +ve i/p terminal at at the point of V_2' shown in figure, we can write,

$$\frac{V_2 - V}{R_1} = \frac{V - V_2'}{R_2} = \frac{V_2' - V_1'}{R_4} + \frac{V_2'}{R_2} \quad \text{---(2)}$$

Deducting (2) from (1) we can write,

$$\frac{V_1 - V_2}{R_1} = \frac{V_2' - V_1'}{R_2} = \frac{V_1' - V_2'}{R_4} \times 2 + \frac{V_1' - V_2'}{R_2} - \frac{V_0}{R_2} \quad \text{---(3)}$$

From 1st two parts of eqn (3), we can write,

$$V_2' - V_1' = \frac{R_2}{R_1}(V_1 - V_2) \quad ---(4)$$

From last two parts of eqn (3), we can write,

$$\frac{V_0}{R_2} = \frac{2(V_1' - V_2')}{R_4} + \frac{(V_1' - V_2') \times 2}{R_2}$$

$$\frac{V_0}{R_2} = 2(V_1' - V_2')\left(\frac{1}{R_2} + \frac{1}{R_4}\right) \quad ---(5)$$

Using the value of $(V_2' - V_1')$ from (4) to (5), we get-

$$\frac{V_0}{R_2} = 2 \times \frac{R_2}{R_1}(V_2 - V_1)\left(\frac{1}{R_2} + \frac{1}{R_4}\right)$$

or, $$\boxed{V_0 = 2\frac{R_2}{R_1}\left(1 + \frac{R_2}{R_4}\right)(V_2 - V_1)}$$

17. Advantages of active filters over passive filters are-
(i) Gain can be increased and can be adjusted,
(ii) circuit reliability will be increased.
(iii) Performance can be improved.
(iv) Design procedure is simpler.
(v) Size and weight can be reduced.

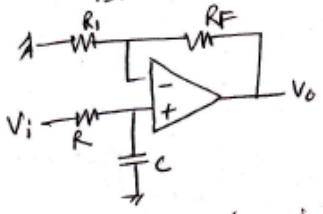
characteristics of Butterworth filter —
Butterworth filter is also called maximally flat or flat-flat filter, which gives closed loop gain close to be one within pass band and roll offs can be steeper approaching to ideal filter more ~~ideally~~ closely. Also, to increase roll off, we can use one OPAMP instead of using 2 (for -40dB/decade roll off) or more (3 for -60dB/decade roll off and so on). Characteristics of Butterworth filter is that it does not keep phase angle constant at cut off frequencies. For a basic LP filter,

following is the characteristics of Butterworth polynomial and its roll off & phase angle –

$B_n(s) = \sqrt{1+\left(\frac{w}{w_0}\right)^{2n}}$ = normalized Butterworth polynomial.
w → operating freq., w_0 = cut-off freq.

order (n)		Roll off	phase angle between o/p & i/p
1	→ $1+s$	– 20dB/decade	-45^0
2	→ $1+\sqrt{2}s+s^2$	– 40dB/decade	-90^0
3	→ $(1+s)(1+s+s^2)$	– 60dB/decade	-135^0
4	→ $(1+0.765s+s^2)(1+1.848s+s^2)$	– 80dB/decade	-180^0

18. 1st order active low-pass filter is shown below –



The dc gain is provided by R_F and R_1 and is $\left(1+\frac{R_F}{R_1}\right)$.
The R-C network at +ve i/p terminal is used to provide the cut-off freq.
The filter is to be designed to get pass-band gain 5 and cut-off freq. 1KHz.

$1+\frac{R_F}{R_1} = 5$ or, $\frac{R_F}{R_1} = 4$

If $R_1 = 1K$, $R_F = 4K$ It is needed to get pass band gain = 5.

Cutoff freq. $= f = \frac{1}{2\pi RC} = 1$ KHz

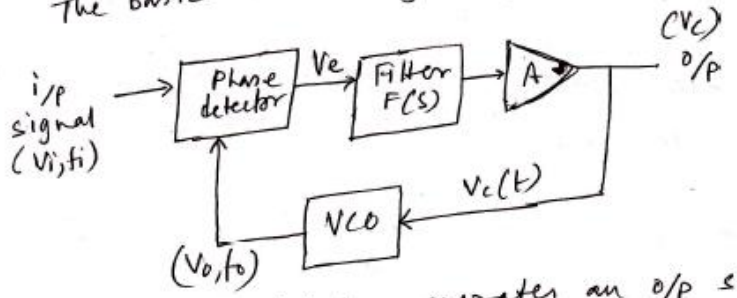
Let $C = 0.1\,\mu F$

Then $R = \frac{1}{2\pi C \times f} = \frac{1}{2\pi \times 0.1\times10^{-6}\times10^{+3}}$

$= 1.59\times10^3\,\Omega$ $= 1.59\,K\Omega$.

$\therefore$ $C = 0.1\,\mu F$, $R = 1.59\,K\Omega$ It is needed to get cut-off freq. of 1 KHz for this low pass filter.

19. PLL is a closed loop feedback system that locks the output frequency and phase to the freq. and phase of an input signal. PLL is generally used to track a carrier or synchronizing signal that may vary in freq. with time. The basic block diagram of PLL is shown below-



The phase detector generates an o/p signal that is a function of the difference in phase between two i/p signals. o/p of phase detector is filtered, amplified and then dc component of error signal is applied at i/p of VCO. VCO o/p freq. is fedback to the phase detector. VCO control voltage Vc(t) forces VCO to change the freq. in the dirⁿ that reduces the differences between i/p freq. and o/p freq. If the two freq. are close, PLL feedback system will force the two i/p freq. of phase detector to be equal and VCO is locked with i/p i.e. fi=fo.

Applications of PLL are as follows-

(1) Freq. multiplication and division,
(2) Amplitude modulation detection,
(3) FM detection,
(4) FSK modulation / demodulation,
(5) Frequency synthesizing,
(6) Satellite Communication application.

20. Resolution of 4-bit DAC is 20 mV/bit.

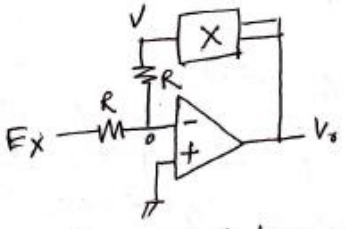
Input is $(1011)_2 = 11|_{\text{decimal}}$

Analog output voltage corresponding to i/p $(1011)_2$ will be $20 \times 11 = 220$ mV.

Input is $(0010)_2 = 2|_{\text{decimal}}$

Analog output voltage corresponding to i/p $(0010)_2$ will be $20 \times 2 = 40$ mV.

21.



Due to closed loop feedback established through the analog multiplier, we can write, voltage at -ve terminal of OPAMP to be zero. Then by using KCL at -ve i/p terminal,

$$\therefore \frac{E_x - 0}{R} = \frac{0 - V}{R} \quad \text{or, } V = -E_x \quad \text{--- (1)}$$

Now, V = o/p voltage of multiplier

V_o = i/p voltage at both terminal of multiplier

Then we can write for multiplier, $V = V_o^2$

$$\text{or, } V_o = \sqrt{V} \quad \text{--- (2)}$$

Using eqn (1) and (2), we can write,

$$V_o = \sqrt{-E_x}$$

If E_x is a -ve voltage, we can write, $E_x = -|E_x|$

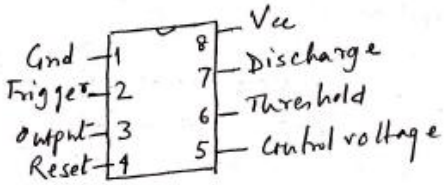
Then, $\boxed{V_o = \sqrt{|E_x|}}$ i.e. a combination of multiplier connected with OPAMP as shown in the above ckt can act as square-root operator.

22. Quantization error of an ADC is the smallest discrete digital output of ADC corresponding to least significant bit of input. If no. of bits of digital output increases, no. of steps will also increase, hence i/p voltage per step will decrease, hence quantization error will decrease.

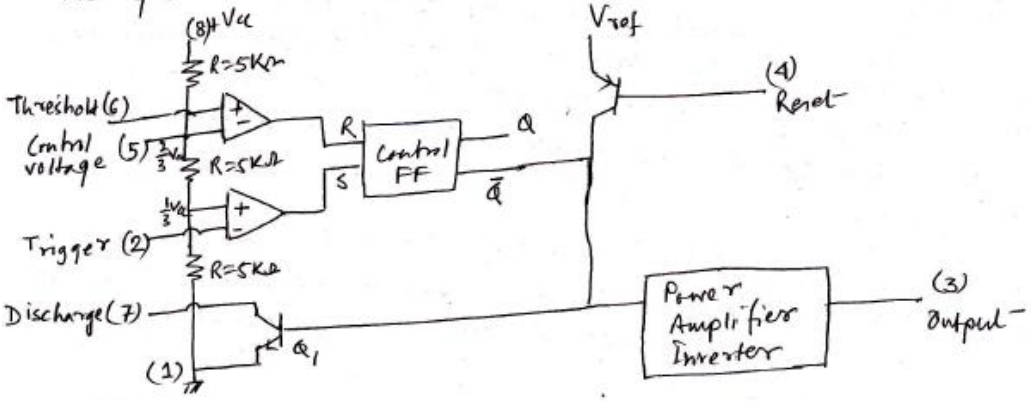
∴ Quantization error of an ADC = $\pm \frac{1}{2}$ LSB.

Resolution of an ADC is defined as the min^{m} change in the input signal which is accepted for conversion. For n-bit ADC, the resolution will be $\frac{1}{2^n}$.

23. The pin configuration of IC-555 timer ckt is given below -



The functional block diagram of IC-555 timer ckt is given below -



In IC-555 timer, 2 ~~components~~ comparators, namely UC (Upper comp.) and LC (Lower comp.) are used. Three 5kΩ resistors provide potential divider arrangement, giving $\frac{2}{3}V_{cc}$ at -ve i/p terminal of UC and $\frac{1}{3}V_{cc}$ at +ve i/p terminal of LC. A control voltage i/p terminal at pin 5 accepts external voltage to control the operation of UC. Operation of IC is ~~summerized~~ summerized as shown in table below-

Status of operation of IC-555

Trigger (Pin 2)	Threshold (Pin 6)	o/p (Pin 3)	Discharge (Pin 7)
$< \frac{1}{3}V_{cc}$	$< \frac{2}{3}V_{cc}$	High	open
$< \frac{1}{3}V_{cc}$	$> \frac{2}{3}V_{cc}$	Last state	Last state
$> \frac{1}{3}V_{cc}$	$< \frac{2}{3}V_{cc}$	Last state	Last state
$> \frac{1}{3}V_{cc}$	$> \frac{2}{3}V_{cc}$	~~Last state~~ Low	Gnd

Stable state makes $\bar{Q}$ = high ∴ making o/p of inverting power amp. low. A -ve going trigger pulse is applied at pin 2, o/p of LC = high. This makes $Q=1$, $\bar{Q}=0$. When threshold voltage at pin 6 is above $\frac{2}{3}V_{cc}$, o/p of UC goes high, making $Q=0$, $\bar{Q}=1$ i.e control FF resets. Reset terminal at pin 4 resets the timer by grounding pin 4 or reducing its voltage level below 0.4V. This makes o/p at pin 3 low overriding the operation of LC. When not used, reset terminal is connected to +Vcc. Q_2 isolates reset i/p from FF & Q_1. Ref. voltage Vref available internally from Vcc. Q_1 acts as discharge transistor when o/p at pin 3 is high, Q_1 = off, & discharge terminal at pin 7 is open. When o/p at pin 3 is low, Q_1 is ON, discharge terminal is short ckt to gnd.

29. The necessary cond^n to generate freq. of oscillation are (1) Barkhausen Criteria of loop gain $AB=-1$ should be maintained where A = gain of forward path, B = Gain of feedback path, (2) Output and input should be of same phase.

The diff. between oscillator & amplifier is that - (1) Amplifier uses -ve feedback & osc. uses +ve feedback. (2) Gain of opamp lies in linear range in case of amplifier while gain is nonlinear in use of oscillator. (3) Amplifier gives stabilization of gain, oscillator not, (4) Amplifier operation reduces nonlinear distortion, oscillator not.